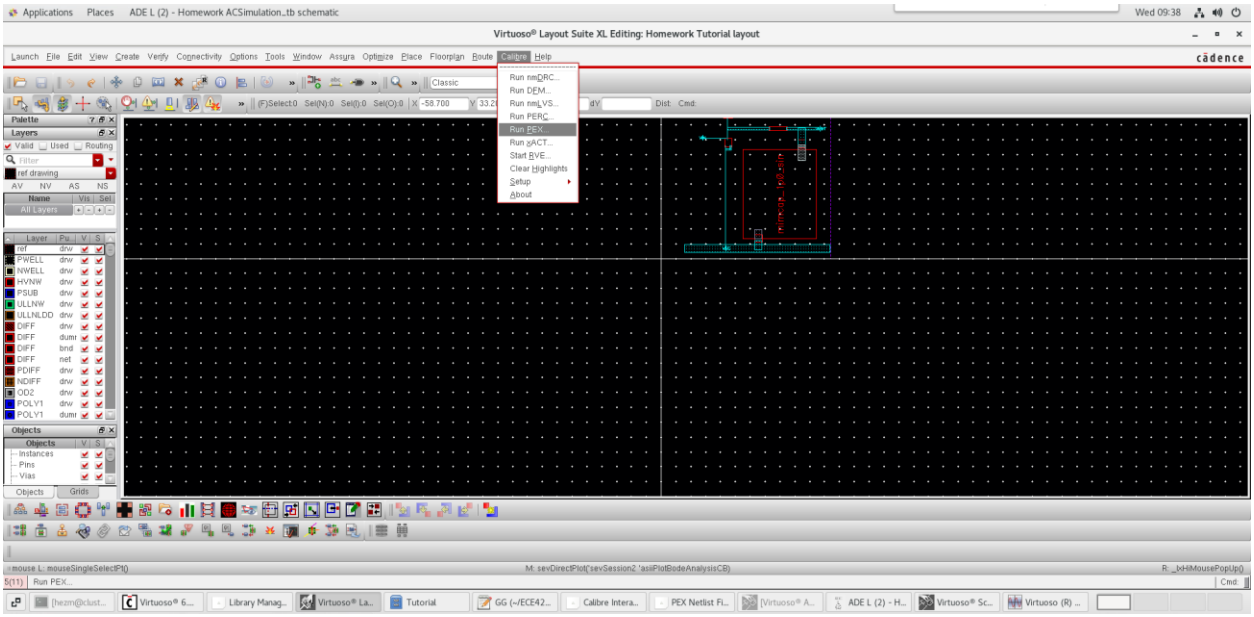
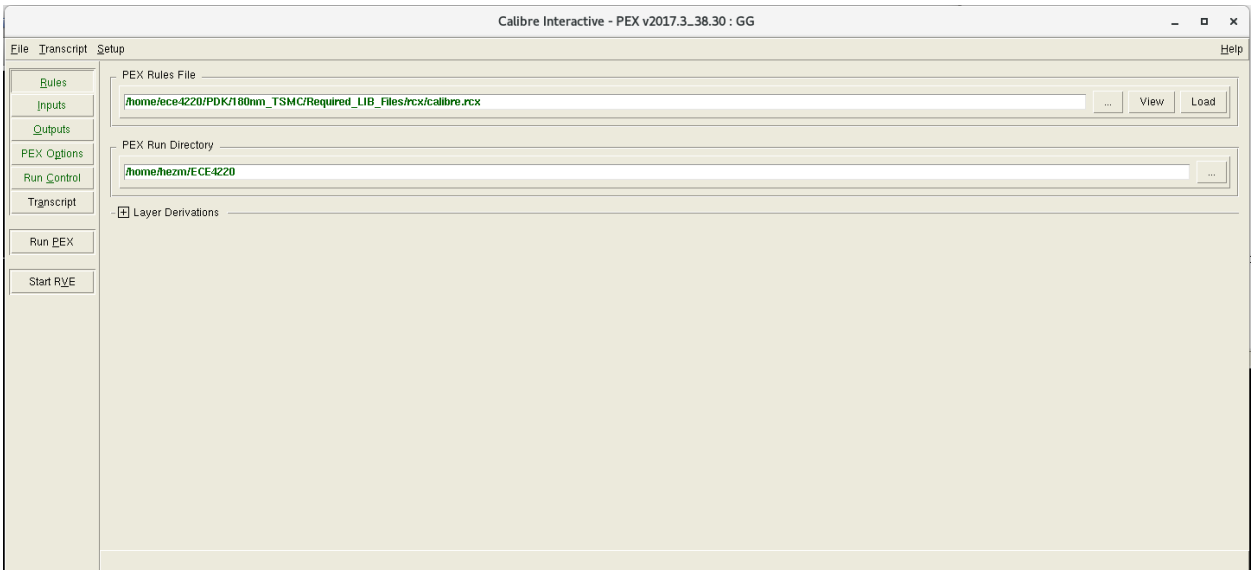
**Parasitic Extraction and Post-Layout Simulation**

Author: Jinhua Wang

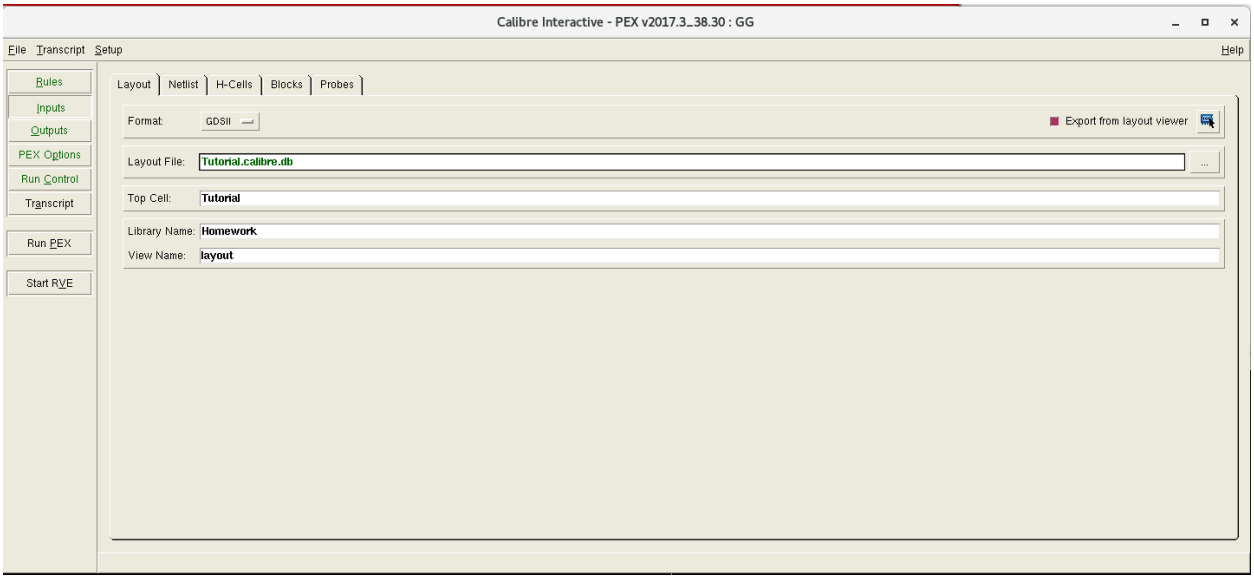
1. PEX is used to generate the parasitic capacitance and resistance of your layout design. Click **Calibre** -> **Run PEX.**



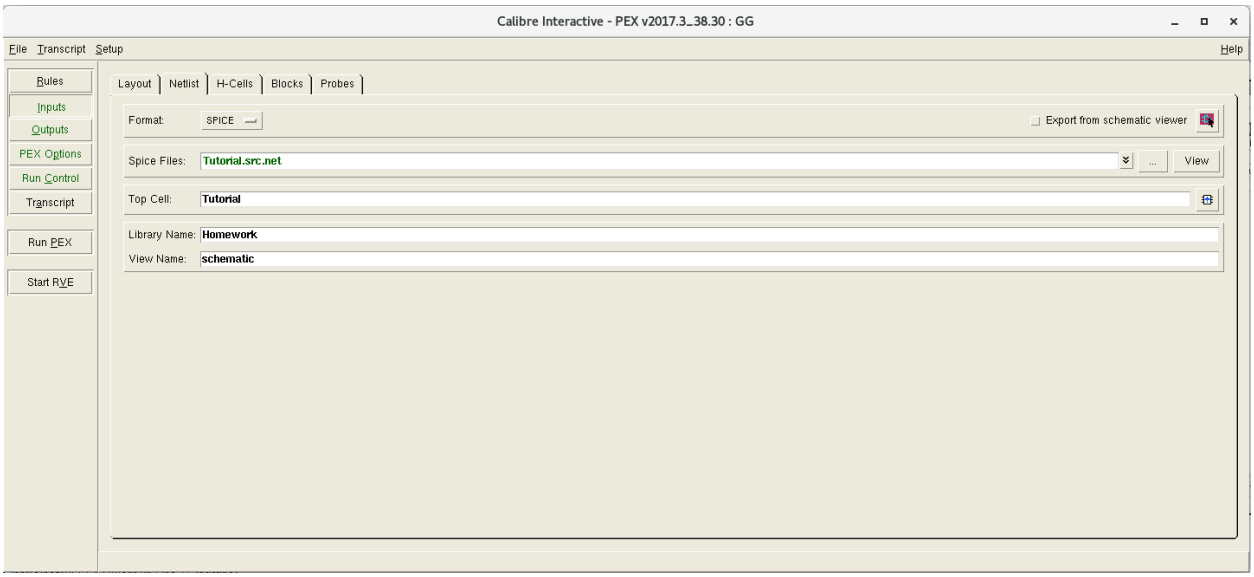

2. Click **Cancel** when the **Load Runset File** window pops up. You may save a **runset** after finishing this tutorial for later use.
3. Set the PEX Rules File path to **/home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calibre.rcx**



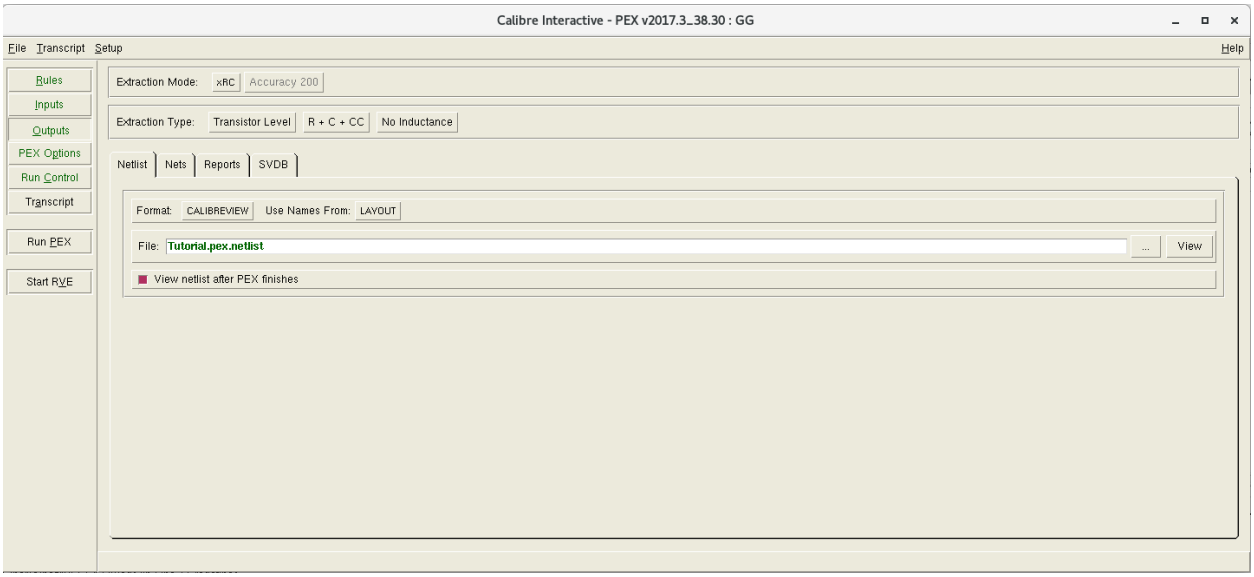
4. In **Inputs**, click **Layout**, make sure the setup is the same as below(with your own cell/library names).




5. In **Inputs**, click **Netlist**, make sure the setup is the same as below (with your own cell/library names).



6. In **Outputs**, click **Netlist**, make sure the setup is the same as below (with your own cell/library names). **R + C + CC** is usually used because it is the closest to the real situation.

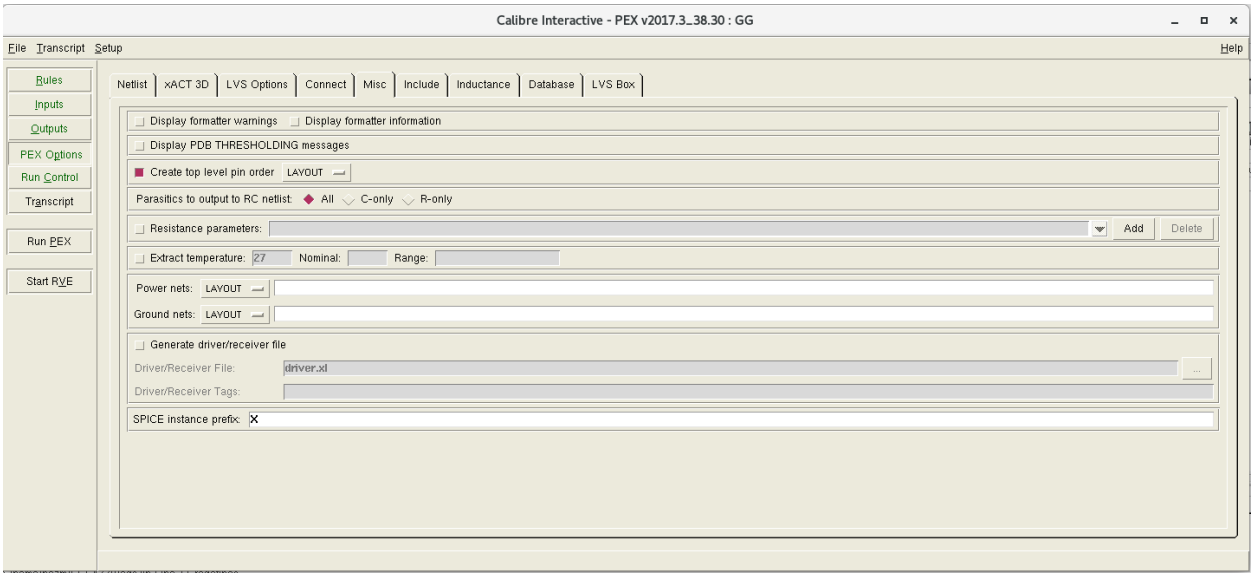



**R**: parasitic resistance

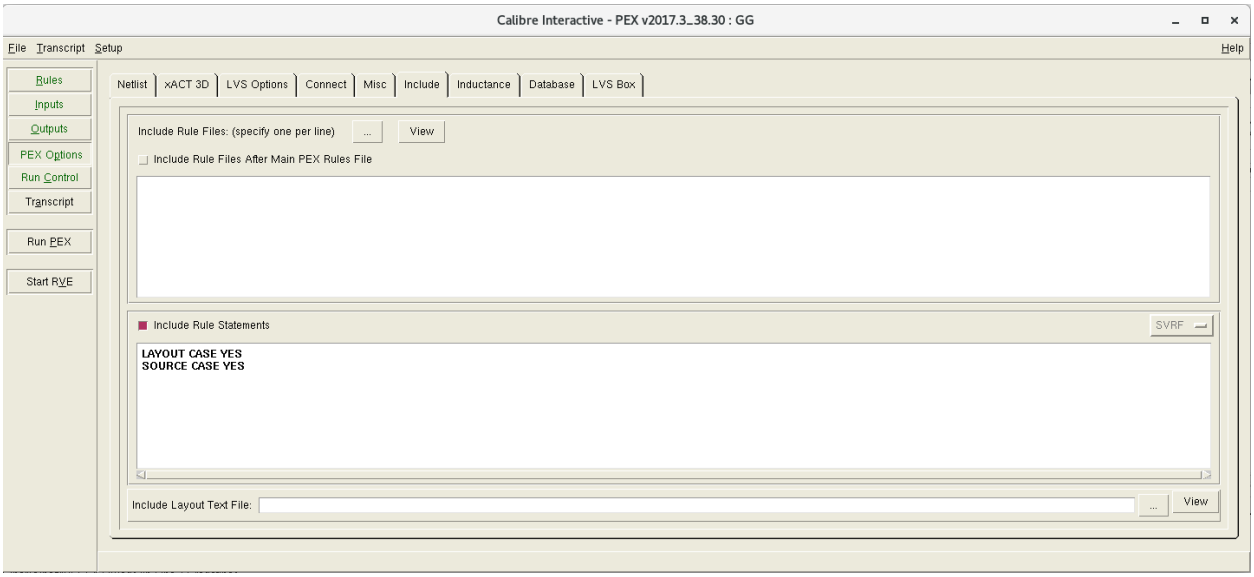
**C**: lumped parasitic capacitance extracted to ground

**CC**: coupling capacitance

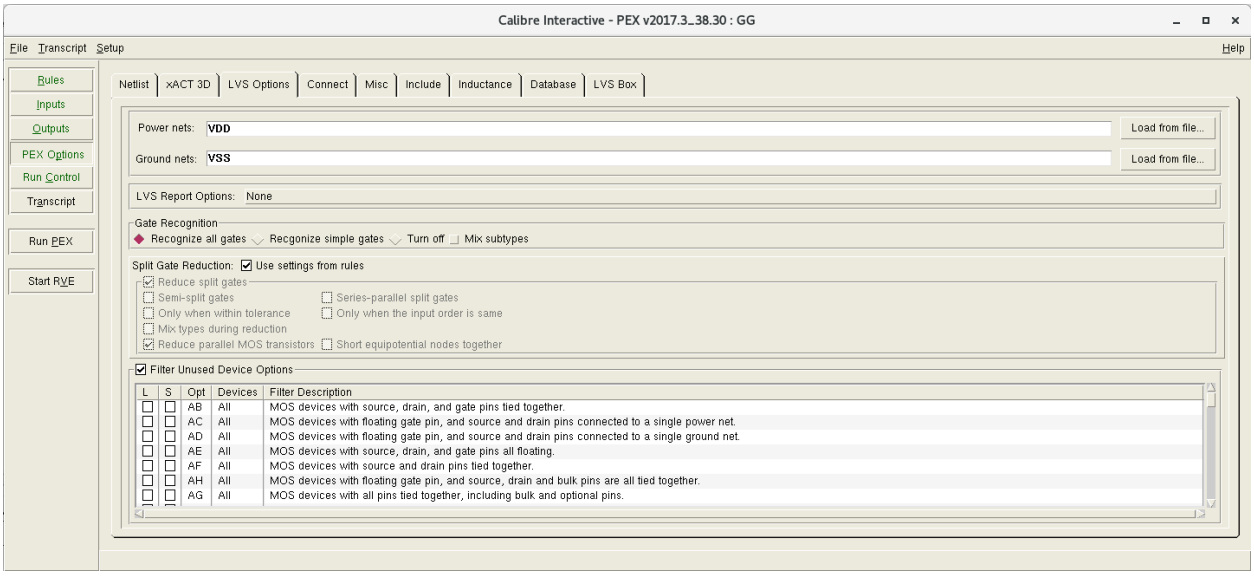
7. Go to **Setup** in the top menu, enable **PEX Options**.
8. In **PEX Options**, go to **Misc**, enable **Create top level pin order** and select **LAYOUT**



9. In **PEX Options**, go to **Include**, enable **Include Rule Statements**, and enter the following commands
   **LAYOUT CASE YES**
   **SOURCE CASE YES**




10. In **PEX Options**, go to **LVS Options**, enter **VDD** for **Power nets**; enter **VSS** for **Ground nets**. (case sensitive)



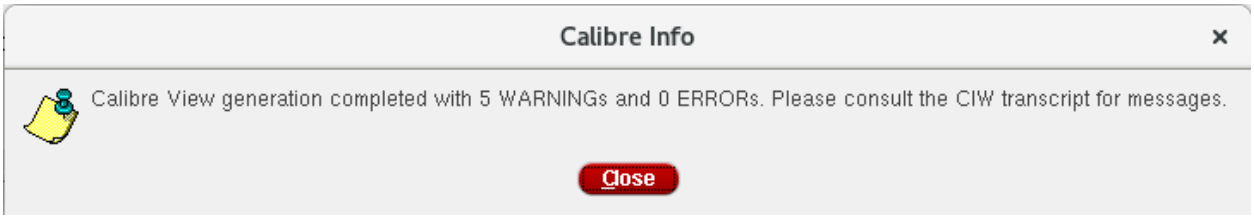

11. After finishing all configurations, click **Run PEX**. A **Calibre view setup** window should pop up. Make sure the **Cellmap File** path is

**/home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calview.cellmap**

Set **Calibre View Type** to **schematic.**

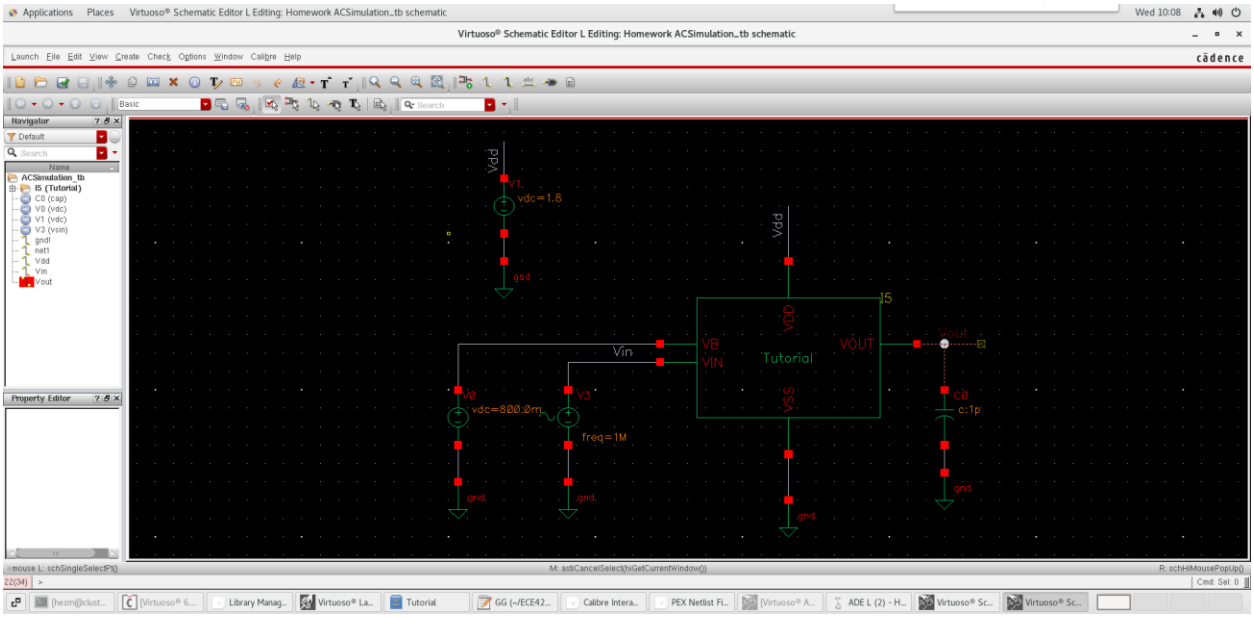
Set **Create Terminals** to **Create all terminals.**


12. Click **OK**. A **Calibre Info** window should pop up, correct the errors if there are any.

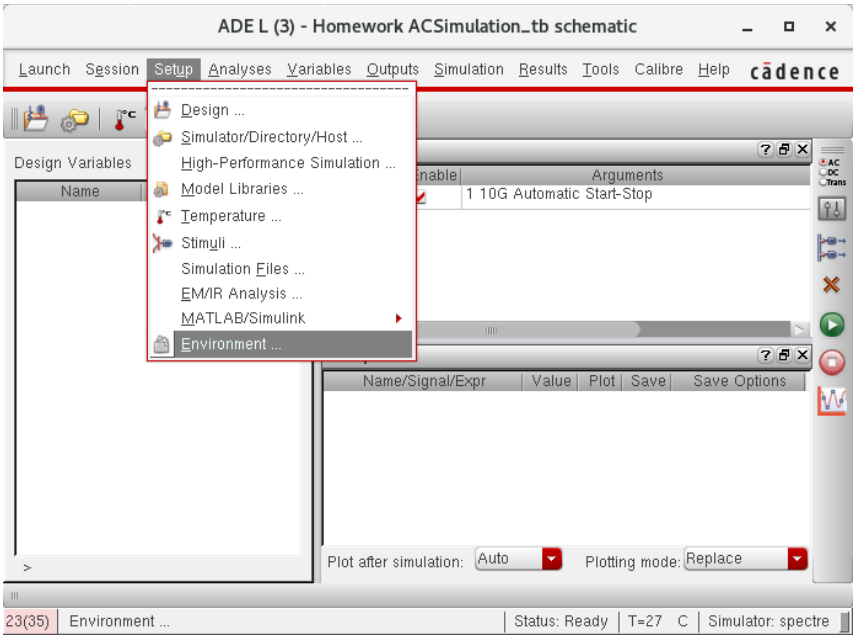



13. Now you have a layout view (**calibre**) with the parasitic capacitance and resistance. You need to do a **post-layout simulation** to compare it with the **front-end simulation** that you did before to see if you need to do any modifications on your design.

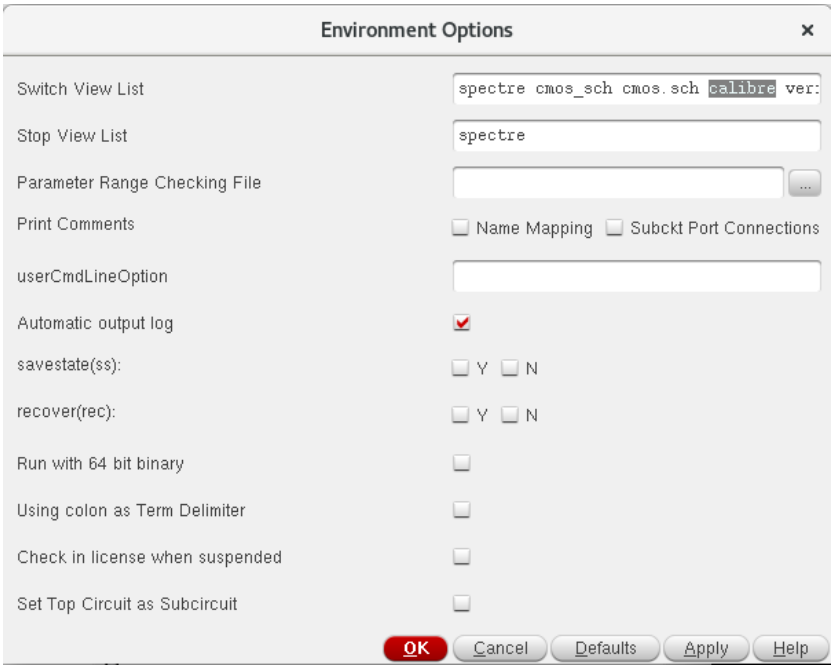
14. Go to the testbench that you previously create for the **front-end simulation**.



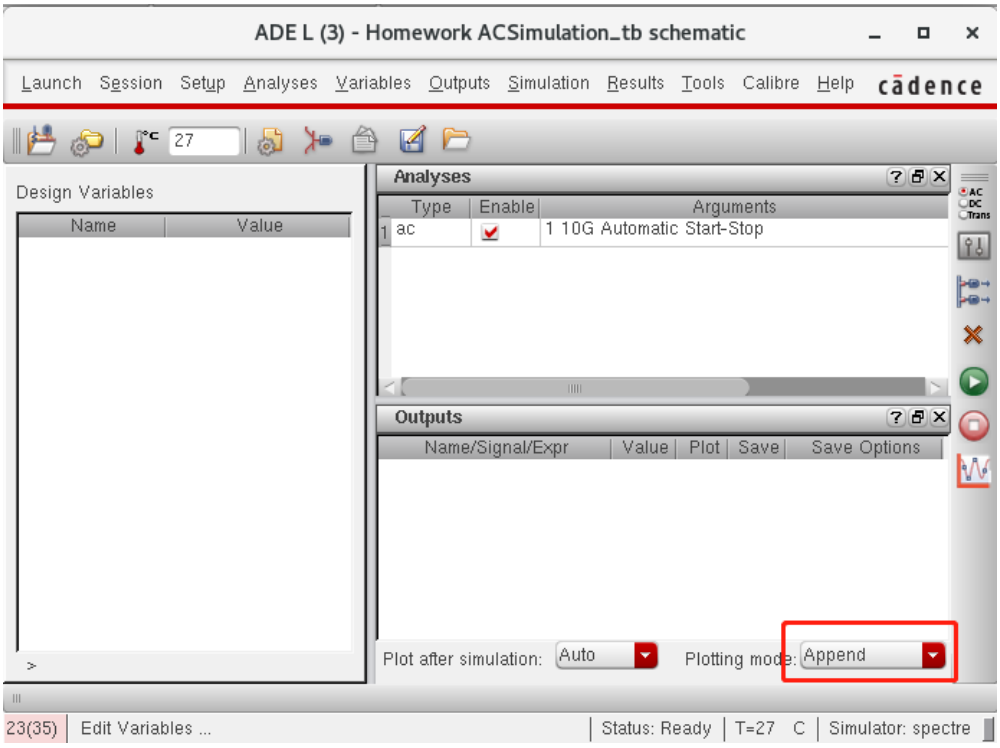

15. Go to **Launch** -> **ADE L**, and set up the simulation. For example, an **AC analysis** from **1 Hz** to **10 GHz**. Click **Netlist and Run** to get an AC analysis plot, which is a **front-end simulation**.
    **Note**: if you do not know how to do so, please refer to the tutorial "**AC Simulation**".
16. In **ADE L**, go to **Setup** -> **Environment**.



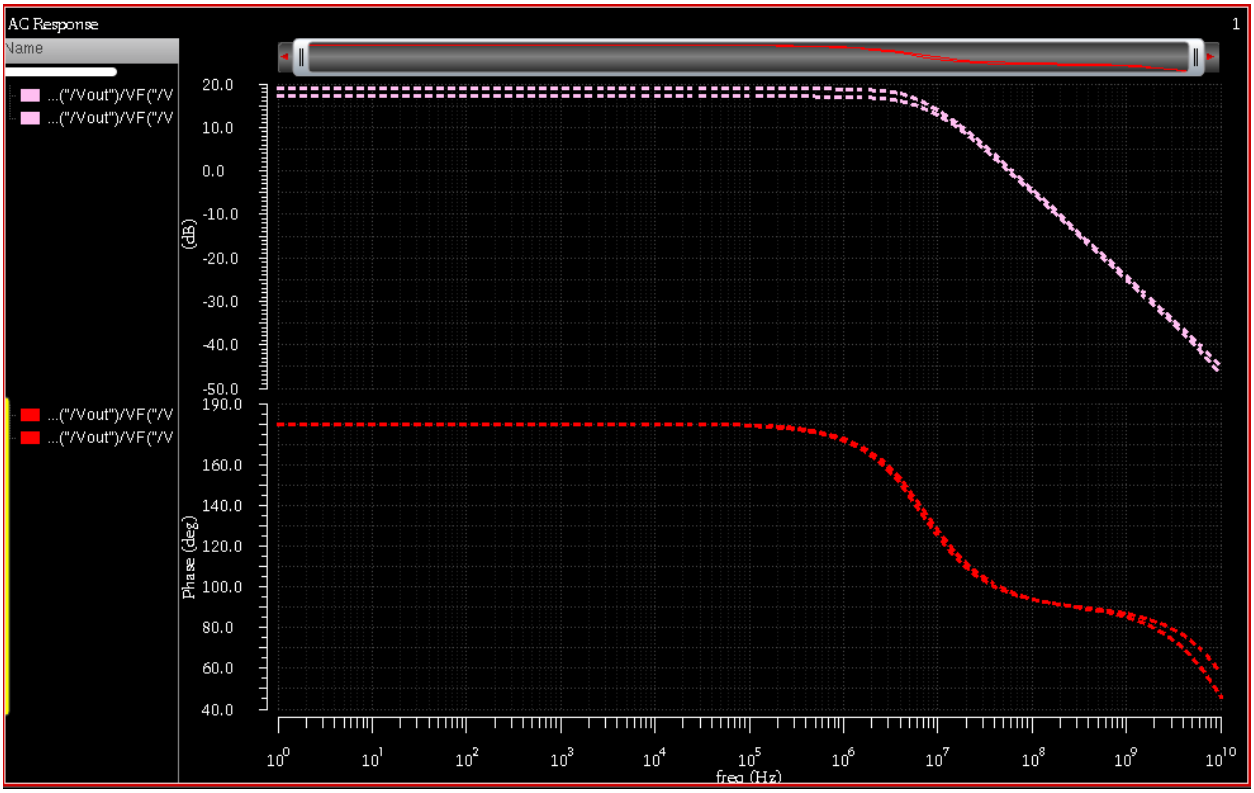
17. Change **schematic** to **calibre**. Click **OK**.




18. In **ADE L**, change **Plotting mode** to **Append**, which makes it easier to observe the error between the front-end simulation and post-layout simulation.



19. Run the simulation and plot it again. The post-layout simulation should be appended to the front-end simulation. If the error cannot be tolerated, modify your layout design.




20. You may save this runset for later use so that you do not need to set it up every time.