Parasitic Extraction and Post-Layout Simulation

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1. PEX is used to generate the parasitic capacitance and resistance of your layout design. Click Calibre -> Run PEX.



- 2. Click **Cancel** when the **Load Runset File** window pops up. You may save a **runset** after finishing this tutorial for later use.
- 3. Set the PEX Rules File path to /home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calibre.rcx

	Calibre Interactive - PEX v2017.3_38.30 : GG	-	в ×
Eile Transcript §	Şelup		Help
Rules	PEX Rules File		
Inputs	/home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calibre.rcx	ViewL	.oad
Outputs	DEV. Due Directory		
PEX Options	PEX Run Directory		
Run <u>C</u> ontrol			
Transcript	- H Layer Derivations		
Run <u>P</u> EX			
Start RVE			

4. In **Inputs**, click **Layout**, make sure the setup is the same as below(with your own cell/library names).

r	Calibre Interactive - PEX v2017.3_38.30 : GG	×
Eile Transcript S	Setup	∐elp
Rules	Layout Netlist H-Cells Blocks Probes	
Inputs	Format GDSII	🔳 Export from layout viewer
PEX Options	Layout File: Tutorial.calibre.db	
Run <u>C</u> ontrol		[
Transcript	Top Cell: Tutonal	
Run PEX	Library Name: Homework	
	View Name: layout	
Start R <u>V</u> E		

5. In **Inputs**, click **Netlist**, make sure the setup is the same as below (with your own cell/library names).

		Calibre Interactive - PEX v2017.3_38.30 : GG	×
Eile Transcript Se	tup	ŧ	leip
Rules	Layout Netlist H-Cells Blocks Probes		
Inputs Outputs	Format: SPICE -	🔟 Export from schematic viewer	
PEX Options Bun Centrol	Spice Files: Tutorial.src.net	3 <u>View</u>	
 Tr <u>a</u> nscript	Top Cell: Tutorial	8	
Run <u>P</u> EX	Library Name: Homework View Name: schematic		
Start RVE			

6. In **Outputs**, click **Netlist**, make sure the setup is the same as below (with your own cell/library names). **R** + **C** + **CC** is usually used because it is the closest to the real situation.

r	Calibre Interactive - PEX v2017.3_38.30 : GG	o x
<u>File</u> <u>T</u> ranscript	Setup	∐elp
Rules	Extraction Mode: xRC Accuracy 200	
Inputs Outputs	Extraction Type: Transistor Level R + C + CC No Inductance	
PEX Options Run <u>C</u> ontrol	Netlist Nets Reports SVDB	
Transcript	Format CALIBREVIEW Use Names From: LAVOUT	
Run <u>P</u> EX	File: Tutorial.pex.netlist	/iew
Start RVE	View netlist after PEX finishes	

R: parasitic resistance

C: lumped parasitic capacitance extracted to ground

CC: coupling capacitance

- 7. Go to **Setup** in the top menu, enable **PEX Options**.
- 8. In PEX Options, go to Misc, enable Create top level pin order and select LAYOUT

	Calibre Interactive - PEX v2017.3_38.30 : GG	• •	×
<u>F</u> ile <u>T</u> ranscript <u>S</u> e	tup	He	elp
Rules	Netlist xACT 3D LVS Options Connect Misc Include Inductance Database LVS Box		
Qutputs PEX Options	Display formatter warnings Display formatter information Display PDB THRESHOLDING messages		
Run <u>C</u> ontrol	Create top level pin order		
Transcript	Parasitics to output to RC netist • All \bigcirc C-only \bigcirc R-only		
Run <u>P</u> EX	Add Dela	te	
Start R <u>V</u> E	Power nets: LAYOUT		
	Generate driver/receiver file		
	Driver/Receiver File: Intriver.xd		
	Driver/Receiver Tags: SPICE instance prefix X	=	
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 In PEX Options, go to Include, enable Include Rule Statements, and enter the following commands LAYOUT CASE YES SOURCE CASE YES

Calibre Interactive - PEX v2017.3_38.30 : GG	×
Elle Iranscript Setup	<u>H</u> elp
Bules Netlist xACT 3D LVS Options Connect Misc Include Inductance Database LVS Box	-)
Qutputs Include Rule Files: (specify one per line) View	
PEX Ogtions	
Hun Control Trgnscript	
Run PEX	
Start RVE	
SVRF -	
LAYOUT CASE YES SOURCE CASE YES	
Include Layout Text File:	

10. In **PEX Options**, go to **LVS Options**, enter **VDD** for **Power nets**; enter **VSS** for **Ground nets**. (case sensitive)

Calibre Interactive - PEX v2017.3_38.30 : GG	_ = ×
Elle Transcript Setup	∐elp
Bules Netlist xACT 3D LVS Options Connect Misc Include Inductance Database LVS Box)
Qutputs Power nets: VDD	Load from file
PEX Options Ground nets: VSS	Load from file
Trgnscript LVS Report Options: None	
Gate Recognition Run <u>PEX</u> • Recognize all gates	
Split Gate Reduction: ☑ Use settings from rules Start RVE ☑ Reduce split gates ☑ Seni-split gates ☑ Series-parallel split gates ☑ Only when within tolerance ☑ Only when the input order is same ☑ Mix Hypes during reduction ☑ Only when the input order is same	
Filter Unused Device Options	
L S Opt Devices Filler Description Image: Ima	

11. After finishing all configurations, click **Run PEX**. A **Calibre view setup** window should pop up. Make sure the **Cellmap File** path is

/home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calview.cellmap

Set Calibre View Type to schematic.

Set Create Terminals to Create all terminals.

	Calibre View Setup
CalibreView Setup File:	
	Browse View Load
CalibreView Netlist File:	/home/hezm/ECE4220/Tutorial.pex.netlist
	Browse
Output Library:	Homework
Schematic Library:	Homework
Cellmap File:	4220/PDK/180nm_TSMC/Required_LIB_Files/rcx/calview.cellmap
	View Edit Browse
Log File:	./calview.log
Calibre View Name:	calibre
Calibre View Type:	🔾 maskLayout 💿 schematic
Create Terminals:	\bigcirc if matching terminal exists on symbol $\ ullet$ Create all terminals
Preserve Device Case	
Execute Callbacks	
Suppress Notes	
Reset Properties:	m=1
Magnify Instances By:	1
Device Placement:	Layout Location
Parasitic Placement:	C Layout Location Arrayed
Show Parasitic Polygons	

12. Click **OK**. A **Calibre Info** window should pop up, correct the errors if there are any.



13. Now you have a layout view (**calibre**) with the parasitic capacitance and resistance. You need to do a **post-layout simulation** to compare it with the **front-end simulation** that you did before to see if you need to do any modifications on your design.



14. Go to the testbench that you previously create for the **front-end simulation**.

- 15. Go to Launch -> ADE L, and set up the simulation. For example, an AC analysis from 1 Hz to 10 GHz. Click Netlist and Run to get an AC analysis plot, which is a front-end simulation. Note: if you do not know how to do so, please refer to the tutorial "AC Simulation".
- 16. In ADE L, go to Setup -> Environment.

	ADE L (3) - H	omework A	CSimulatio	n_tb scl	hemati	c		- 0	×
Launch Session	Set <u>up A</u> nalyses <u>V</u> aria	bles <u>O</u> utputs	<u>S</u> imulation	<u>R</u> esults	<u>T</u> ools	Calibre	<u>H</u> elp	cāder	ce
Design Variables	 Design Simulator/Directory/H High-Performance Si Model Libraries Temperature Stimuli Simulation Eiles EM/R Analysis MATLAB/Simulink Environment 	lost mulation Name/Sig	nable 1 10G gnal/Expr nal/Expr	Automatic	Argu c Start-S	ments Stop Save	Save (? # × ? # × ? # × Options	Coc of the second
23(35) Environme	nt			Status: R	eady	T=27 C	Simu	ilator: spec	tre

17. Change schematic to calibre. Click OK.

Environment Options 2				
Switch View List	spectre cmos_sch cmos.sch calibre ver:			
Stop View List	spectre			
Parameter Range Checking File				
Print Comments	🔲 Name Mapping 🔲 Subckt Port Connections			
userCmdLineOption				
Automatic output log	⊻			
savestate(ss):	🗌 Y 🛄 N			
recover(rec):	🗌 Y 🛄 N			
Run with 64 bit binary				
Using colon as Term Delimiter				
Check in license when suspended				
Set Top Circuit as Subcircuit				
	Cancel Defaults Apply Help			

18. In **ADE L**, change **Plotting mode** to **Append**, which makes it easier to observe the error between the front-end simulation and post-layout simulation.

ADE L (3) -	Homework ACSimulatio	n_tb schematic	_ = ×
<u>L</u> aunch S <u>e</u> ssion Set <u>u</u> p <u>A</u> nalyses <u>V</u> ari	ables <u>O</u> utputs <u>S</u> imulation	<u>R</u> esults <u>T</u> ools Cal	^{ibre <u>H</u>elp cādence}
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			×
			<u>></u>
	Outputs Name/Signal/Expr	Value Plot Sav	el Save Options
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`>	Plot after simulation: Auto	Plotting mo	ode: Append
23(35) Edit Variables		Status: Ready T=27	7 C Simulator: spectre 📕

19. Run the simulation and plot it again. The post-layout simulation should be appended to the front-end simulation. If the error cannot be tolerated, modify your layout design.



20. You may save this runset for later use so that you do not need to set it up every time.