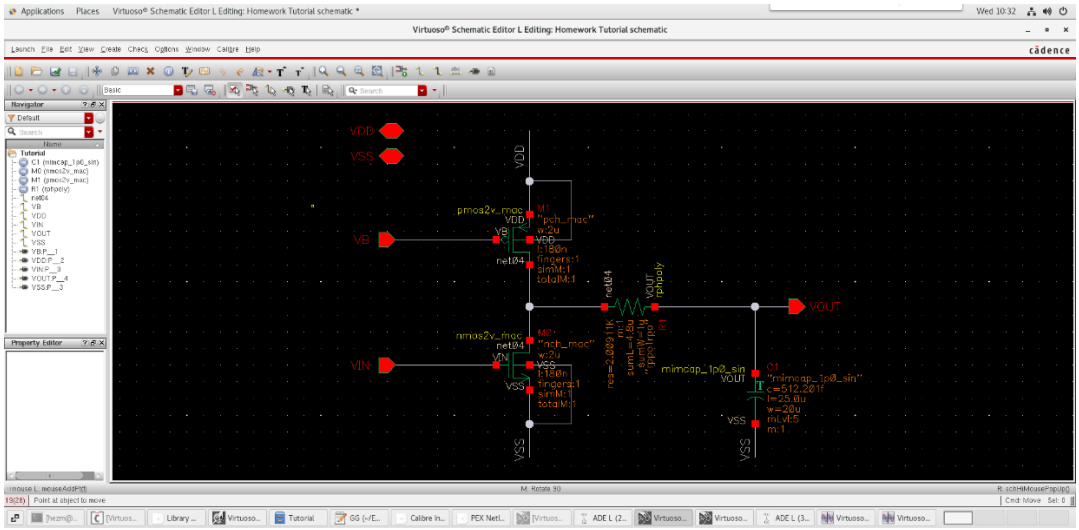
**Layout Component Placement and Routing**

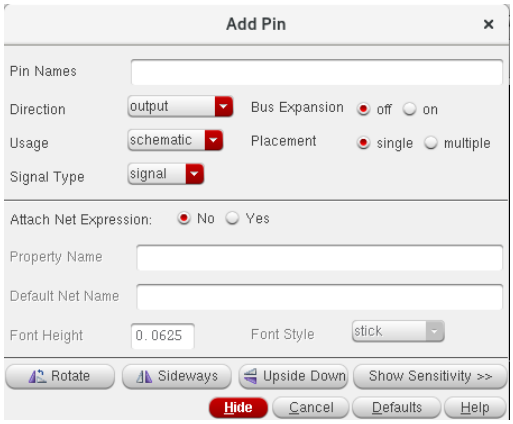
Author: Jinhua Wang

1. Open **Cadence** and create a **schematic view** as below.



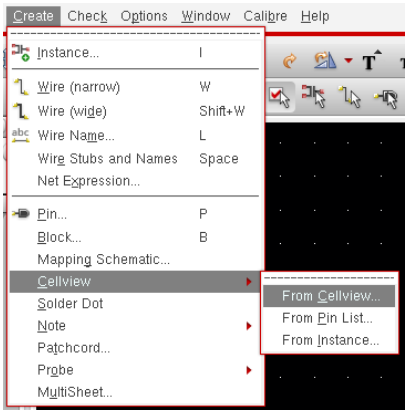

   a. To create a **Pin**, click **Create Pin** in the tool bar


   b. Name the **Pin** (**upper-case** preferred) that you need and make sure the **Direction** is correct.
   **VDD**: inputOutput
   **VSS**: inputOutput
   **VIN**: input
   **VOUT**: output
   Incorrect pin direction will not cause any errors, but only some warnings. For simple circuit, it does not really matter. But as the circuit gets more complicated, it is important to have right pin directions.

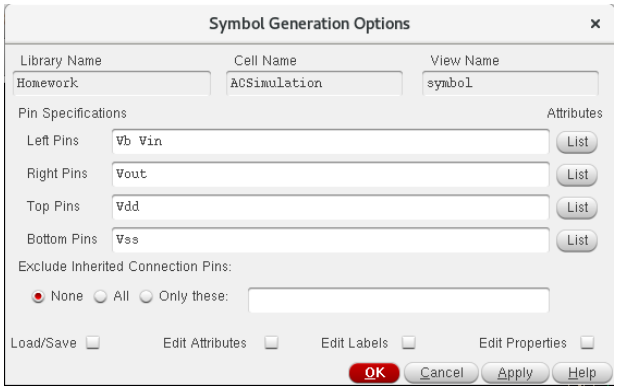


c. For resistors and capacitors, the **ideal** ones from **analogLib** cannot be used anymore. Instead, you need to use **real** cap/res from **tsmc18** library. You need to adjust the **width/length** of the instances to adjust their **resistance/capacitance**.
**Resistor**: rphpoly
**Capacitor**: mimcap_1p0_sin
You may use different components for resistors and capacitors.

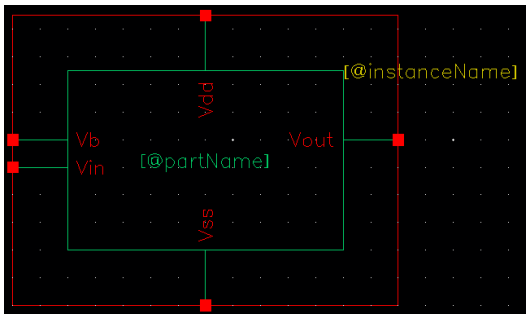
2. After you finish building the schematic, you need to create a **Symbol** out of this schematic.
   **a.** Click **Create** -> **Cellview** -> **From Cellview**



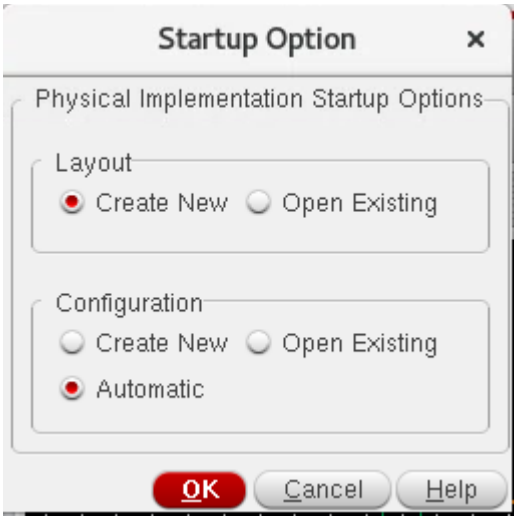

   b. A window should pop up, click **OK**.
   c. Set it up as below, click **OK**.

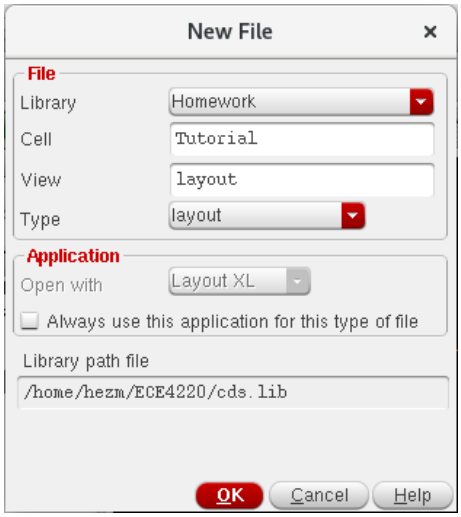



   d. A **Symbol** should be created successfully, which can be used for simulation. The shape can be changed, you may figure it out by yourself if you want to.

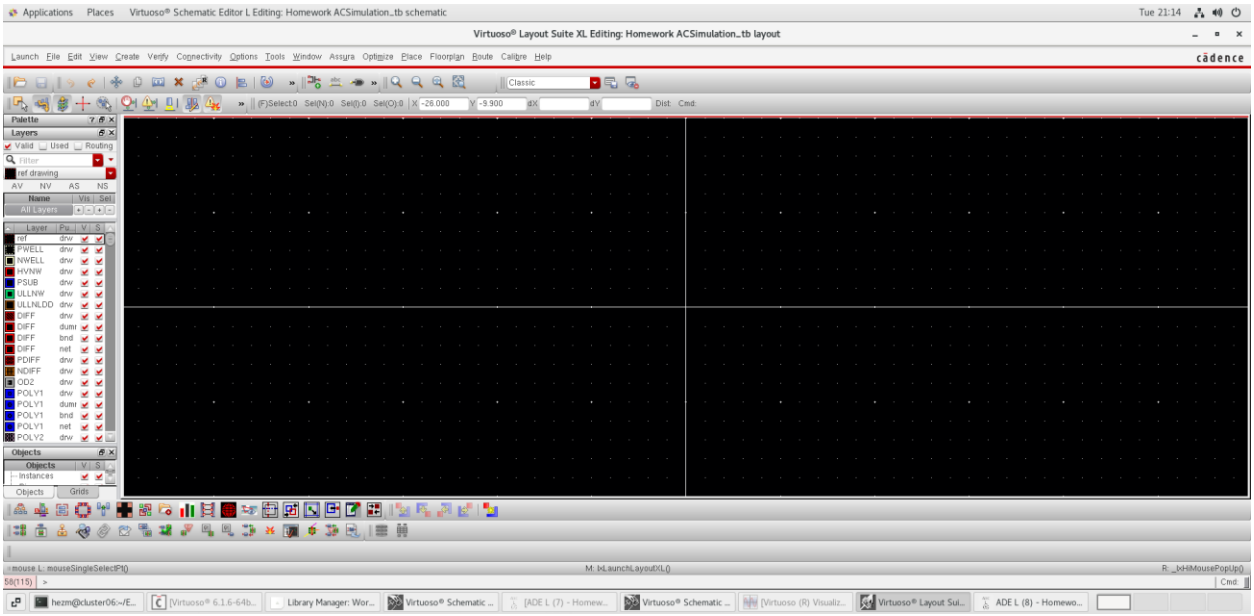


3. After you finish the schematic and create a symbol out of it, do a quick AC analysis to make sure the schematic works fine.
4. After you verify your circuit, click **Launch** -> **Layout XL**. Set up the options as below, and click **OK**.

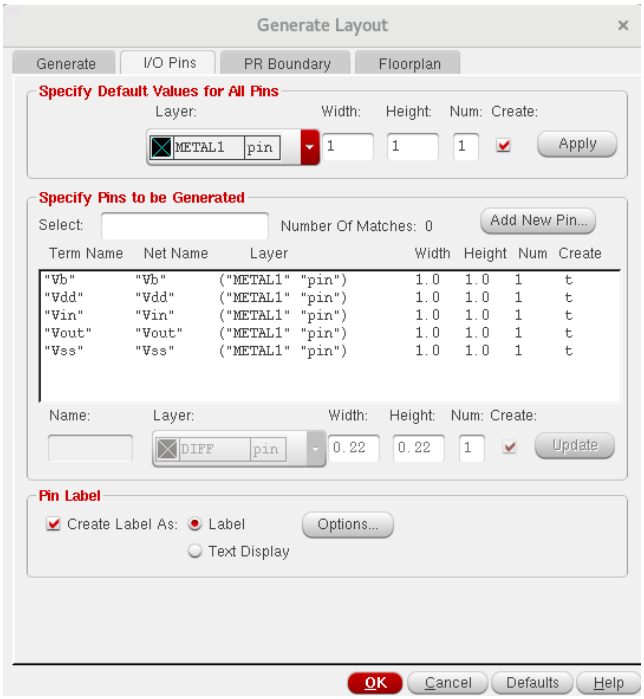



5. If it asks about the **License Info**, click **Yes**.
6. A window of **Layout Suite XL Editing** should pop up.

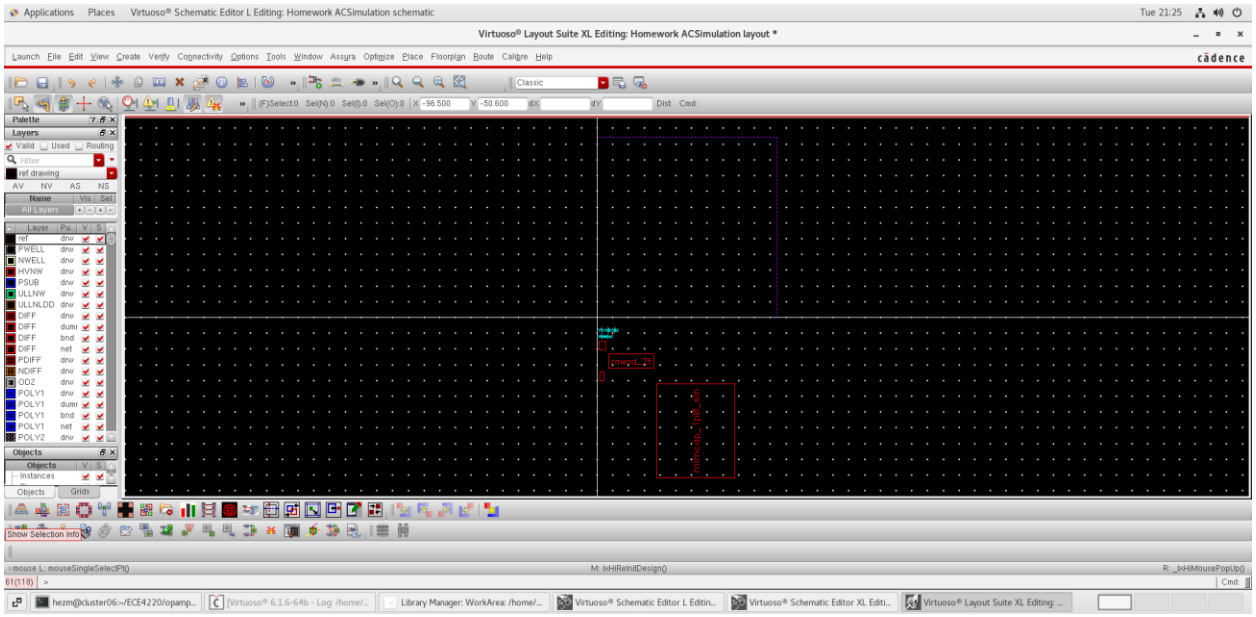


7. In the Virtuoso XL layout menu, click **Connectivity -> Generate -> All From Source…**
    a. Go to **I/O Pins**, set **Layer** to **METAL1 pin**, **width** to **1**, **Height** to **1** and click **Apply**.

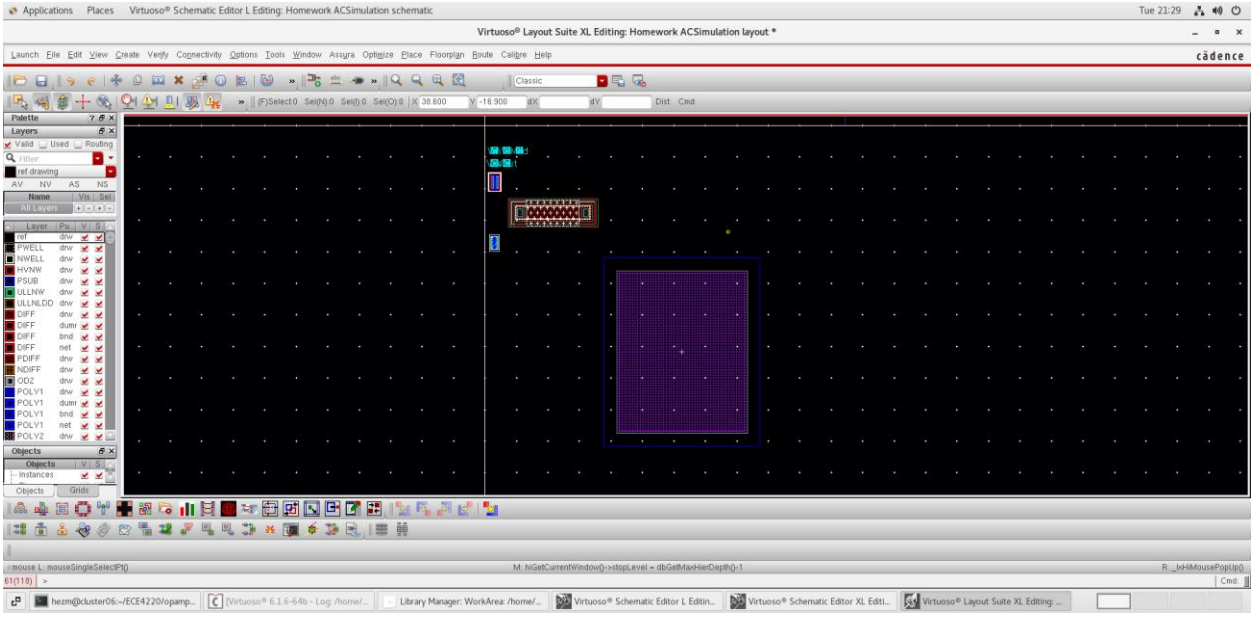



    b. Under **Pin Label**, enable **Create Label As**, and select **Label**, click **Options**. Set up the **Options** as below and click **OK**.

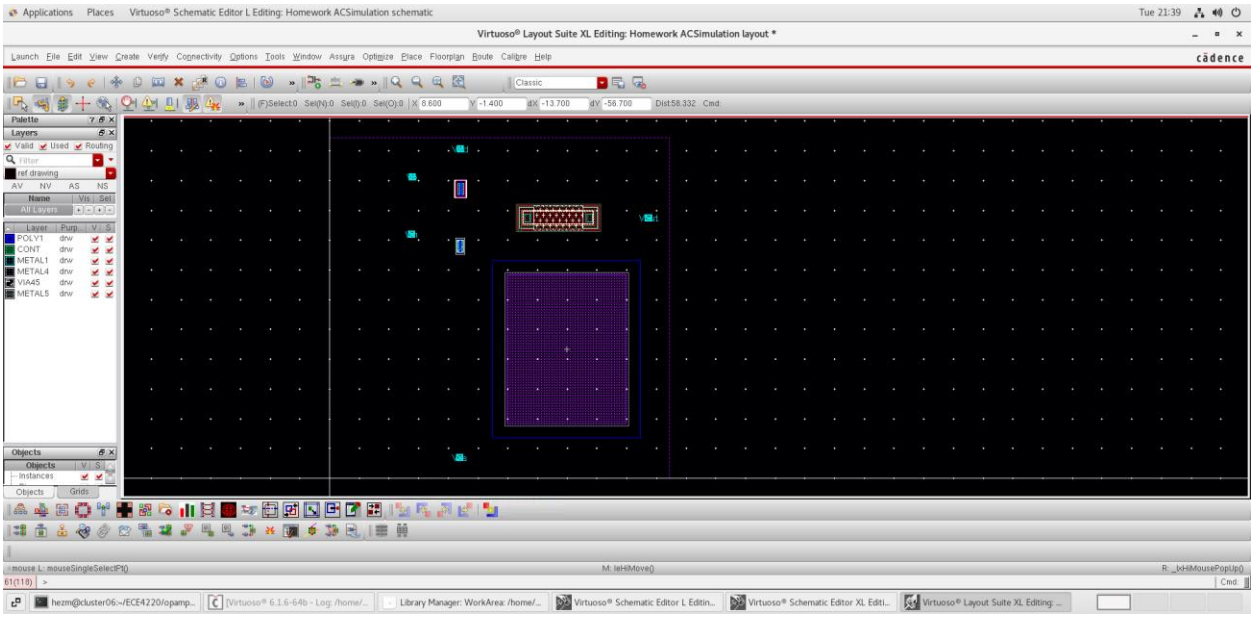
8. All **Components/Pins** should appear in the editor window.



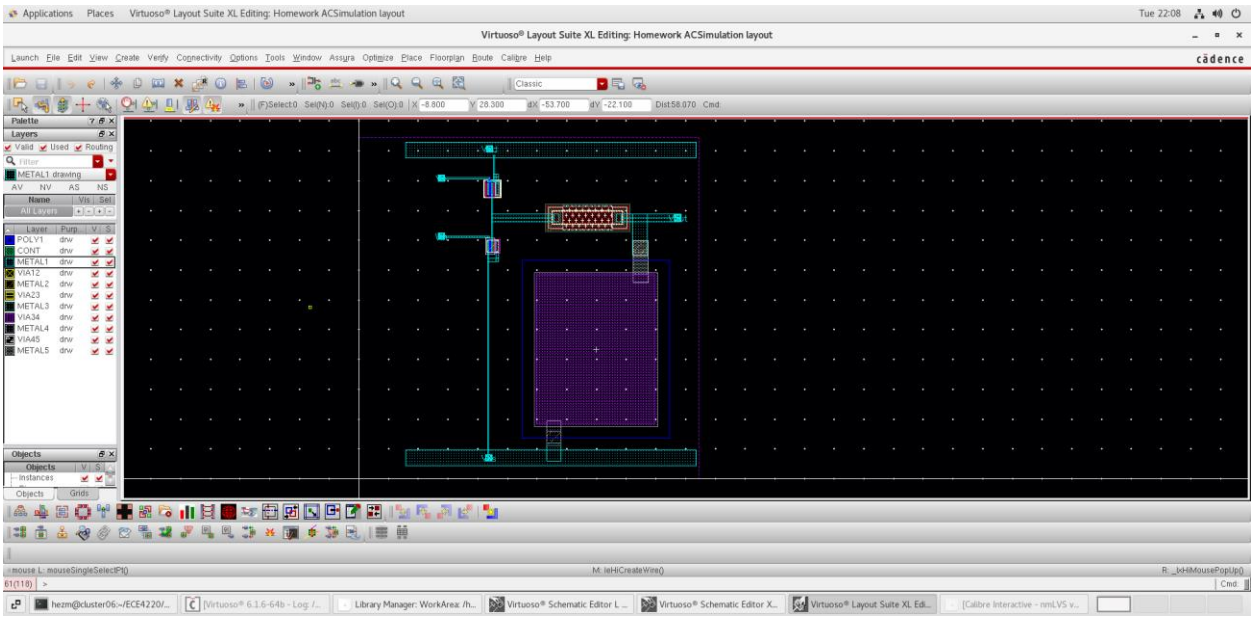

9. Press **shift + f** to see the actual component.



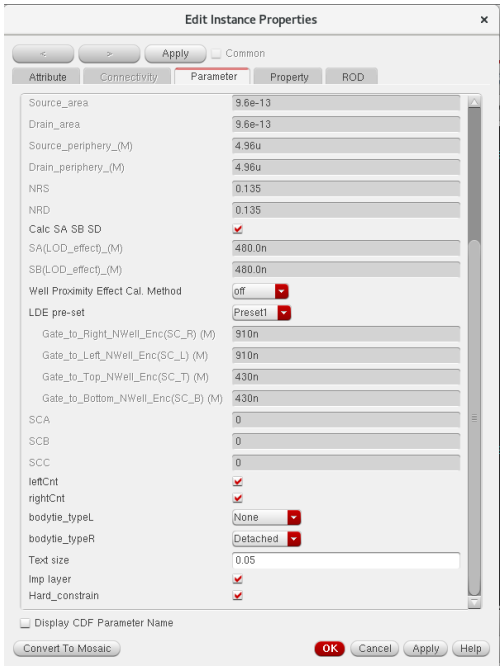
10. Move **all Pins/Components** into the **purple box** above and place the **Pins/Components** the way you want. Try to make the routing **as short as possible**.




11. In this tutorial, **metal 1 (M1)** will be used to do the major routing.
    a. To see the **air wires (guiding wires)**, click **Connectivity** -> **Nets** -> **Show/Hide All Incomplete Nets**.
    b. Press **P** to create **path** (small area).
    c. Press **R** to create **rectangle** (large area).
    d. Press **O** to insert **Via**.
        i. Via is used to connect two different layers.
12. The complete layout should look like below.

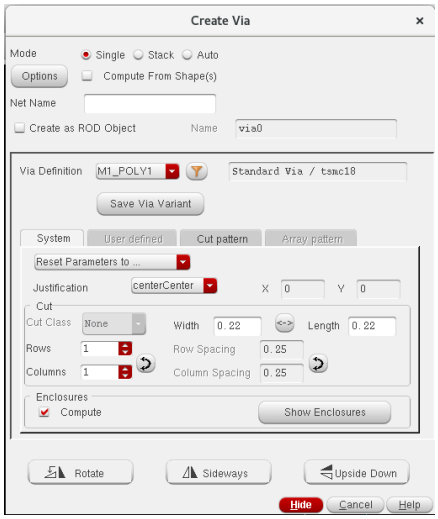


a. Make sure the **Body terminal** for both NMOS and PMOS is connected to the proper potentials. To enable **Body terminal**,
    i. **Right-click** on the MOS instance and click **Properties**.
    ii. Go to **Parameter**, scroll down, and find **bodytie_typeR**/**bodytie_typeR.**
    iii. Set **either one** (not both) to **Detached**.

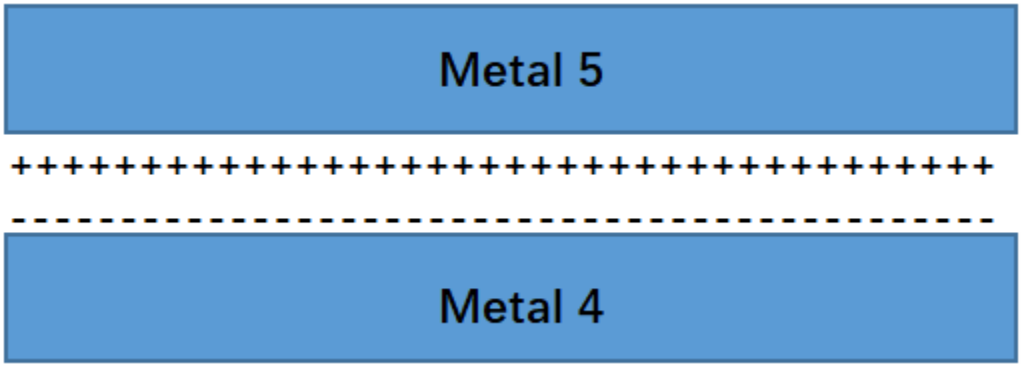



b. The **Gate** of MOS should be connected with **POLY** (**blue path**), which means that a **Via** (**poly to M1**) should be used to connect the **Pin to Gate**. Press **O** and set **Via Definition** to **M1_POLY1**. You may change the size of the Via by changing the number o**f Rows** and **Columns.**

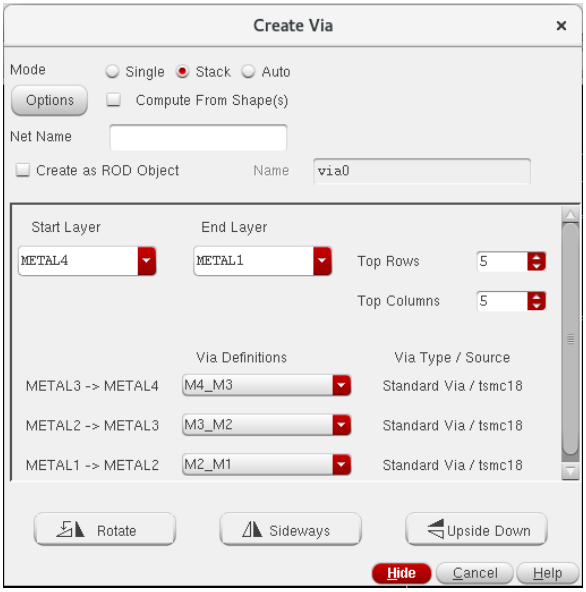
**Note**: you should not change the **Width** and **Length** of the Via to change the size of it, which will cause errors in DRC.



c. The two terminals of the **MIM capacitor** in **tsmc18** is defined as (not polarized),




i. So you need **two Vias**, one is **M5 to M1** and the other is **M4 to M1** to connect the two terminals of the capacitor.
ii. Press **O** to insert Via, change **Mode** to **Stack**.
iii. Set the **Start Layer** and **End Layer**.




13. After the layout is finished, it needs to pass **Design Rule Check** (DRC) and **Layout Vs. Schematic** (LVS) and also do **Parasitic Extraction** (PEX), which will be introduced in the following tutorials.