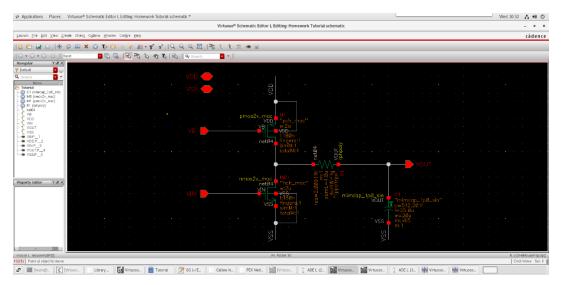
Layout Component Placement and Routing

Author: Jinhua Wang

1. Open **Cadence** and create a **schematic view** as below.



a. To create a Pin, click Create Pin in the tool bar

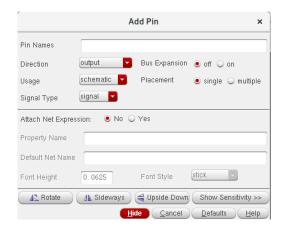


b. Name the **Pin** (**upper-case** preferred) that you need and make sure the **Direction** is correct.

VDD: inputOutput VSS: inputOutput VIN: input

VOUT: output

Incorrect pin direction will not cause any errors, but only some warnings. For simple circuit, it does not really matter. But as the circuit gets more complicated, it is important to have right pin directions.

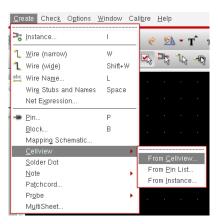


c. For resistors and capacitors, the ideal ones from analogLib cannot be used anymore. Instead, you need to use real cap/res from tsmc18 library. You need to adjust the width/length of the instances to adjust their resistance/capacitance. Resistor: rphpoly

Capacitor: mimcap_1p0_sin

You may use different components for resistors and capacitors.

- 2. After you finish building the schematic, you need to create a **Symbol** out of this schematic.
 - a. Click Create -> Cellview -> From Cellview



- b. A window should pop up, click **OK**.
- c. Set it up as below, click **OK**.

	S	ymbol Gene	ration Option	15	×
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Pin Specificatio	ons				Attributes
Left Pins	Vb Vin				List
Right Pins	Vout				List
Top Pins	Vdd				List
Bottom Pins	Vss				List
Exclude Inherit	ed Connection Pin	\$:			
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Load/Save 📃	Edit Attrib	utes 📃	Edit Labels		Edit Properties 📃
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d. A **Symbol** should be created successfully, which can be used for simulation. The shape can be changed, you may figure it out by yourself if you want to.

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- 3. After you finish the schematic and create a symbol out of it, do a quick AC analysis to make sure the schematic works fine.
- 4. After you verify your circuit, click **Launch** -> **Layout XL**. Set up the options as below, and click **OK**.

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OK Cancel Help		<u>O</u> K <u>C</u> ancel	<u>H</u> elp

- 5. If it asks about the License Info, click Yes.
- 6. A window of Layout Suite XL Editing should pop up.

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7. In the Virtuoso XL layout menu, click Connectivity -> Generate -> All From Source...
a. Go to I/O Pins, set Layer to METAL1 pin, width to 1, Height to 1 and click Apply.

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b. Under **Pin Label**, enable **Create Label As**, and select **Label**, click **Options**. Set up the **Options** as below and click **OK**.



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8. All **Components/Pins** should appear in the editor window.

9. Press **shift + f** to see the actual component.

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10. Move all Pins/Components into the purple box above and place the Pins/Components the way you want. Try to make the routing as short as possible.

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- 11. In this tutorial, **metal 1 (M1)** will be used to do the major routing.
 - a. To see the air wires (guiding wires), click Connectivity -> Nets -> Show/Hide All Incomplete Nets.
 - b. Press P to create path (small area).
 - c. Press **R** to create **rectangle** (large area).
 - d. Press **O** to insert **Via**.
 - i. Via is used to connect two different layers.
- 12. The complete layout should look like below.

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- a. Make sure the **Body terminal** for both NMOS and PMOS is connected to the proper potentials. To enable **Body terminal**,
 - i. Right-click on the MOS instance and click Properties.
 - ii. Go to Parameter, scroll down, and find bodytie_typeR/bodytie_typeR.
 - iii. Set either one (not both) to Detached.

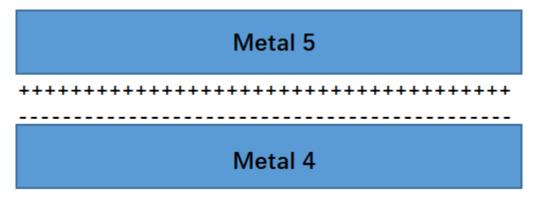
Edit Ins	tance Properties ×
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Source_area	9.6e-13
Drain_area	9.6e-13
Source_periphery_(M)	4.96u
Drain_periphery_(M)	4.96u
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SA(LOD_effect)_(M)	480.0n
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LDE pre-set	Preset1
Gate_to_Right_NWell_Enc(SC_R) (M)	910n
Gate_to_Left_NWell_Enc(SC_L) (M)	910n
Gate_to_Top_NWell_Enc(SC_T) (M)	430n
Gate_to_Bottom_NWell_Enc(SC_B) (M)	430n
SCA	0 =
SCB	0
SCC	0
leftCnt	✓
rightCnt	⊻
bodytie_typeL	None
bodytie_typeR	Detached 🔽
Text size	0.05
Imp layer	⊻
Hard_constrain	✓
Display CDF Parameter Name	
Convert To Mosaic	OK Cancel Apply Help

b. The Gate of MOS should be connected with POLY (blue path), which means that a Via (poly to M1) should be used to connect the Pin to Gate. Press O and set Via Definition to M1_POLY1. You may change the size of the Via by changing the number of Rows and Columns.

Note: you should not change the **Width** and **Length** of the Via to change the size of it, which will cause errors in DRC.

Create Via	×
Mode Single Stack Auto Options Compute From Shape(s) Net Name Create as ROD Object Name via0	
Via Definition MI_POLV1 Via / taxc18 Save Via Variant System User defined Cut pattern Array, pattern Reset Parameters to	
Justification CenterCenter X 0 Y 0	
Cut Cut Class None • Width 0.22 😂 Length 0.2 Rows 1 5 Row Spacing 0.25 Columns 1 5 Column Spacing 0.25	2
Enclosures Show Enclosures	
Rotate	Down

c. The two terminals of the MIM capacitor in tsmc18 is defined as (not polarized),



- i. So you need **two Vias**, one is **M5 to M1** and the other is **M4 to M1** to connect the two terminals of the capacitor.
- ii. Press **O** to insert Via, change **Mode** to **Stack**.
- iii. Set the Start Layer and End Layer.

	Create	Via	×
	Stack O Auto te From Shape(s) Name	via0	
Start Layer	End Layer		
METAL4	METAL1	Top Rows 5 🗧	
		Top Columns 5	
	Via Definitions	Via Type / Source	
METAL3 -> METAL4	M4_M3	Standard Via / tsmc18	
METAL2 -> METAL3	M3_M2	Standard Via / tsmc18	
METAL1 -> METAL2	M2_M1	Standard Via / tsmc18	
E Rotate	Sidew	ays Upside Down	lp

After the layout is finished, it needs to pass Design Rule Check (DRC) and Layout Vs.
 Schematic (LVS) and also do Parasitic Extraction (PEX), which will be introduced in the following tutorials.