Simulation of a Differential Amplifier

Author: Jinhua Wang, Nate Turner, Joseph Chong

1. First navigate to your directory

   cd /home/<Your CVL account name>/ECE4220

```
[hezm@cluster04 ECE4220]$ cd /home/hezm/ECE4220/
[hezm@cluster04 ECE4220]$
```

2. Create a new folder “a1”

```
[hezm@cluster04 ECE4220]$ mkdir a1
```

Note: Make sure the folder name is “a1”. Otherwise the Cadence library manager will not recognize the library name.

3. Copy the necessary files to the folder that you just create by entering the command below

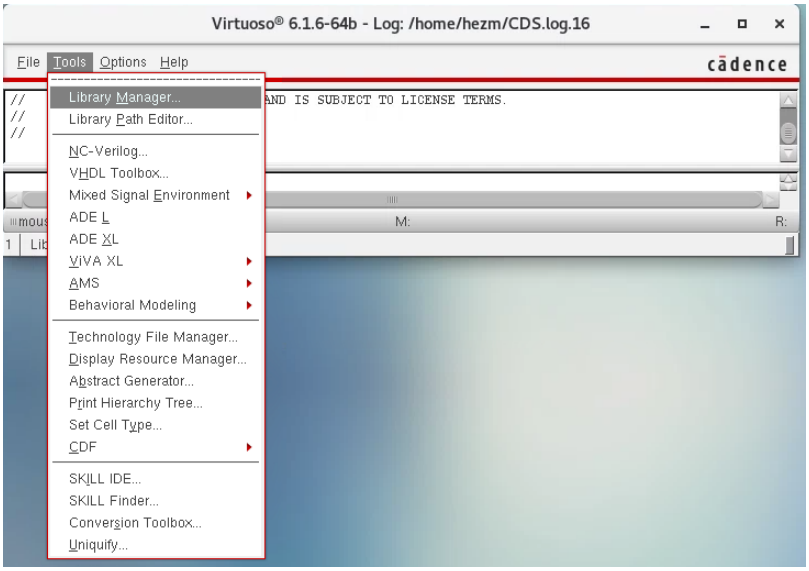
   cp -a /home/ece4220/PDK/180nm_TSMC/a1/. ./

```
[hezm@cluster04 a2]$ cp -a /home/ece4220/PDK/180nm_TSMC/a1/. ./
```

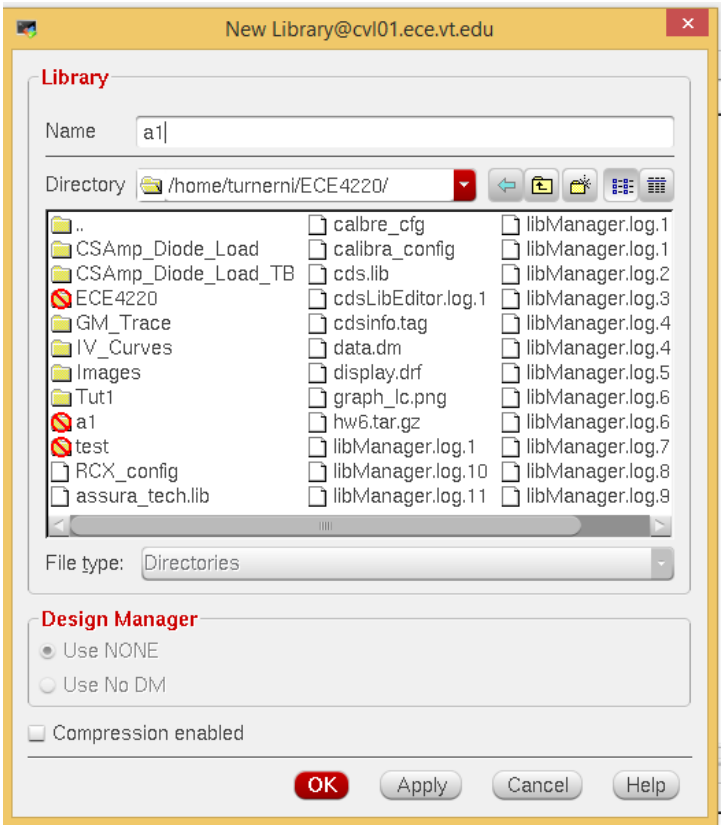
4. Launch Cadence 6.1.6

```
[hezm@cluster04 ECE4220]$ Cadence616
[Cadence616] bash-4.2$ virtuoso &
[1] 7162
[Cadence616] bash-4.2$
```

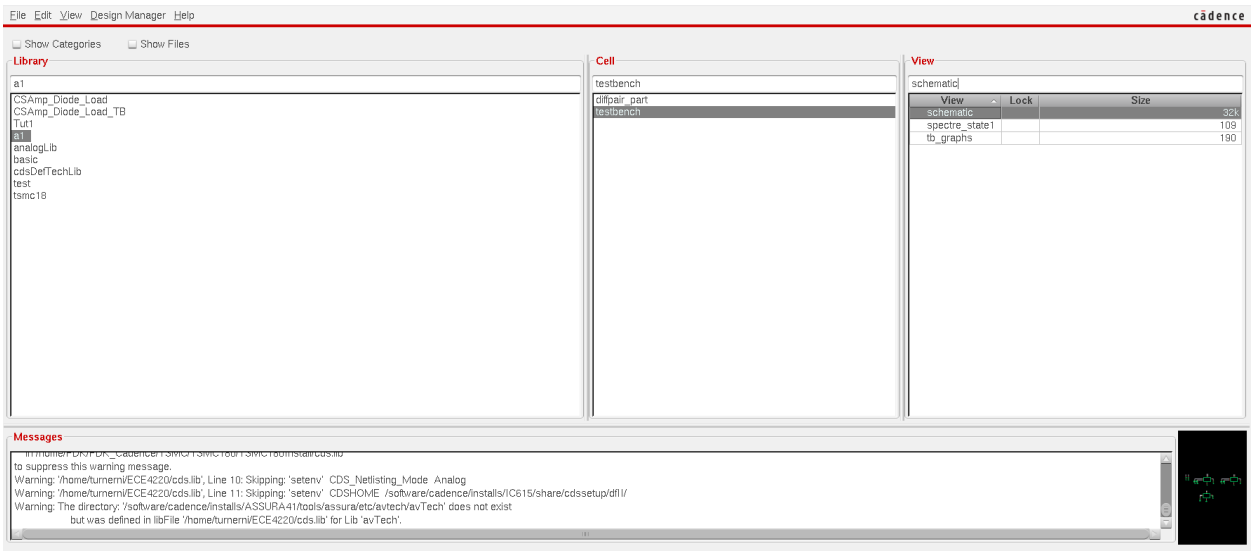
5. In the CIW go to Tools → Library Manager



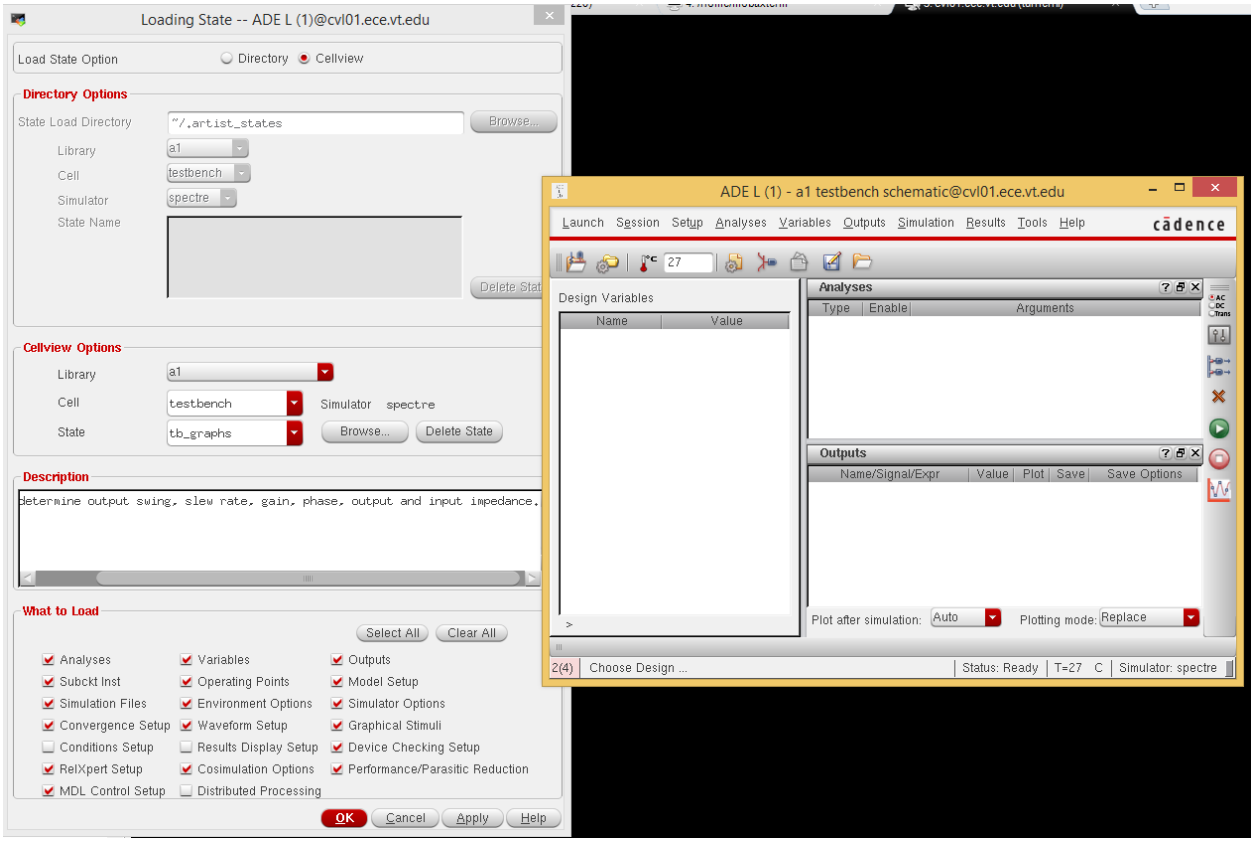
6. Once in the Library Manager go to File → New → Library
7. In the Name Field type “a1” and click OK → Attach to Existing Technology → Select tsmc18



8. Now go to the library you just create and open the testbench cell

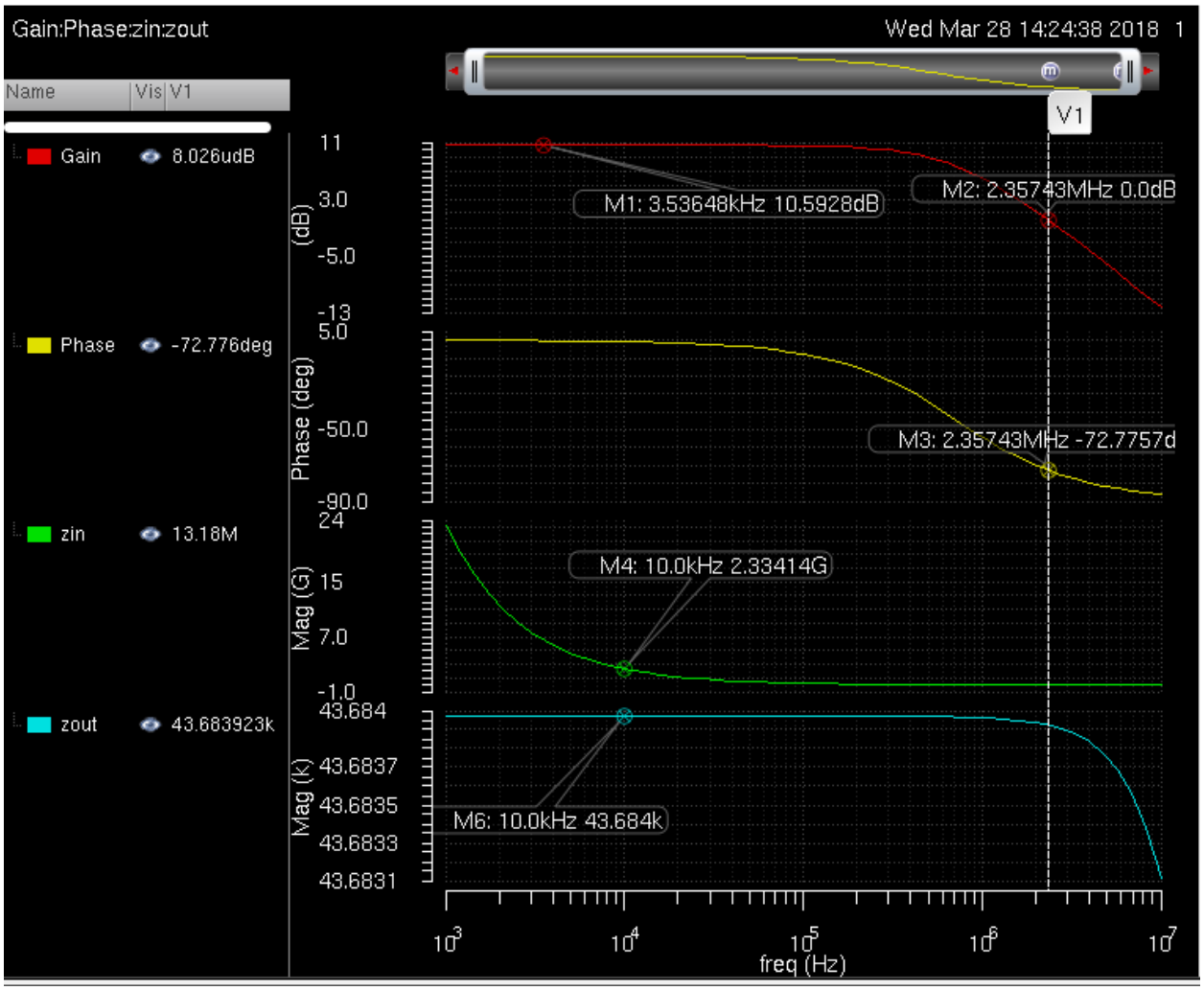


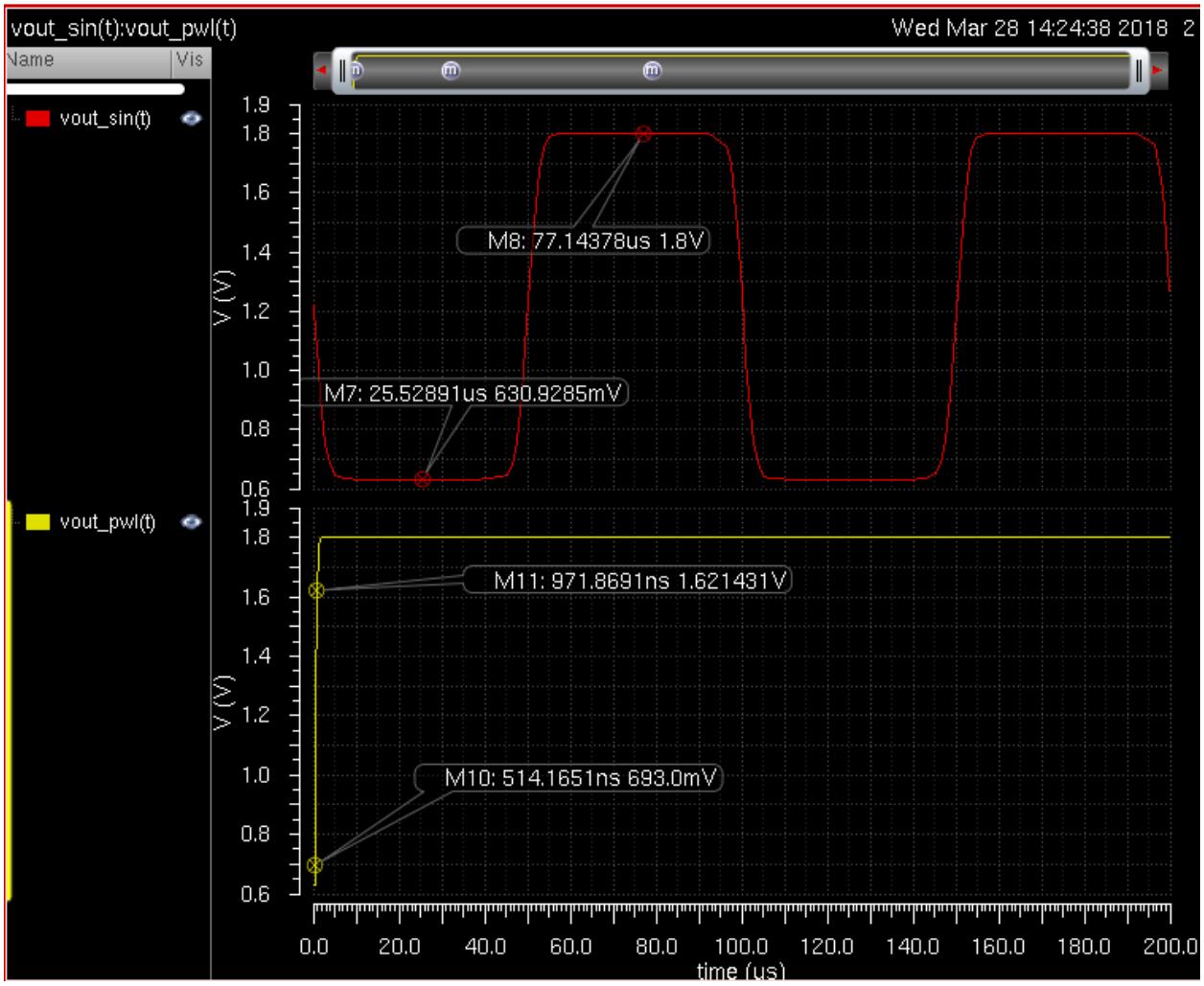
9. Once the schematic has opened go to Launch → ADE L → Session → Load State → Check the Cellview circle → Change State to tb_graphs → Select OK



10. Click Netlist and Run (green arrow) in the ADE
11. The Gain and Phase are the top two graphs, you can place a marker at the 0 dB crossing of the Gain, record that frequency and place another marker at that frequency on the Phase plot to get the phase margin. Phase margin would just be 180 + Phase(G=0 dB) = 180 -72.7757 =~ 107 degrees
12. The bottom two graphs show the magnitude of the input and output impedance.
13. The vout_sin(t) graph can be used to determine the output swing. Just place minimum and maximum markers to determine the values
14. The vout_pwl(t) graph can be used to determine the slew rate. We can define the slew rate as the time is takes for the output voltage to rise from 10% above the minimum to 90% of the maximum output i.e. Vout_min(t)*1.1 to 0.9*Vout_max(t). For this example the calculation would be

$$SR = \frac{0.9V_{DD} - 1.1V_{out,min}}{\Delta t} = \frac{2V}{\mu s}$$


Gain:Phase:zin:zout
Wed Mar 28 14:24:38 2018 1
Name
Vis
V1
Gain
8.026udB
Phase
-72.776deg
zin
13.18M
zout
43.683923k
V1
M1: 3.53648kHz 10.5928dB
M2: 2.35743MHz 0.0dB
M3: 2.35743MHz -72.7757d
M4: 10.0kHz 2.33414G
M6: 10.0kHz 43.684k
11
3.0
-5.0
-13
(dB)
5.0
-50.0
-90.0
Phase (deg)
24
15
7.0
-1.0
Mag (G)
43.684
43.6837
43.6835
43.6833
43.6831
Mag (k)
freq (Hz)



15. if you want to edit the amplifier values you will need to open the schematic view of "diffpair_part" under the "a1" Library.