Dummy Metal Filling

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Before the design is ready to be sent to a foundry for fabrication, there is one last thing to do, which is the dummy metal filling. The dummy metal filling for a CS amplifier is used as an example in this tutorial.

1. Create a new folder under your working directory. You may do it with either the GUI or command lines.



2. Extract the GDS file of the layout that you want to fill the dummy metal on and save it to the folder that you just create.

Note: if you do not know how to do so, please refer to "11_GDS File Extraction".



3. Copy the dummy metal filling script to the folder that you just create. And now you should have two files under the folder.

Note: for different PDKs and different environment setups, the location of the script may differ. If you cannot find the script, talk to the TA.

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🔂 Home		
Documents	CS amplifier ada Dummi Matal	
🕹 Downloads	Calibre_0.18um.214a	
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- 4. Open the file "Dummy_Metal_Calibre_0.18um" and scroll down all the way the Environment Setup part (pink words).
- 5. Setup the environment as below and **Save**.

Open COpen Cop	Save	Ξ	×
// // ENVIRONMENT SETUP //			
LAYOUT SYSTEM GDSII LAYOUT PATH "/home/hezm/ECE4220/dummy_metal_filling/CS_amplifier.gds" LAYOUT PRIMARY "CS_amplifier" LAYOUT PROCESS BOX RECORD YES			
<pre>//Please do not stream-in directly if the topcell name is the same as the original DRC RESULTS DATABASE "dummy_CS_amplifier.gds" GDSII //DRC RESULTS DATABASE "DM.gds" GDSII_DM DRC SUMMARY REPORT "DRC_dummy_CS_amplifier!.sum" DRC MAXIMUM RESULTS ALL DRC KEEP EMPTY NO //LAYOUT ALLOW DUPLICATE CELL YES // allow multiple records for the same layout ce //LAYOUT ERROR ON INPUT NO</pre>	one.		
//****** User defined chip area **********************************	.p window .p window window	1	
VARIABLE yRT 0.0 // y-coordinate of right-top corner for user defined chip LAYER ChipWindow 500 // layer number for constructing chip boundary //******* Options for chip corner empty area definition ************************************	window		
<pre>#DEFINE dmOnCorner // Allow pattern on chip corner? (apply to cell or macro l //#DEFINE BigDieCorner // Corner empty area for big die is used? //#DEFINE WITABEALTING // Already with the sealring structure assembled? //#DEFINE MIXED_SCHEME // Set output data type of DMx as "1". The default output //#DEFINE RFSWITCH // for RFSWITCH process //#DEFINE_Sealring_MonCSR_//_Sealring_without_CSR_structure_(for_RESWITCH_applicat C Tab Width: 8 Ln 21</pre>	data typ ion only 2, Col 43	e is	"0". INS

LAYOUT PATH: the path of the layout that you want to fill the dummy metal on **LAYOUT PRIMARY**: the top cell name of the layout that you want to fill the dummy metal on

DRC RESULTS DATABASE: a dummy metal layout that the script generates (this name must be different from the layout that you want to fill the dummy metal on) **DRC SUMMARY REPORT**: a report that the script generates

6. Open Terminal under this folder, and enter commands,

calibre -drc Dummy_Metal_Calibre_0.18um.214a

[hezm@cluster04 dummy_metal_filling]\$ calibre -drc Dummy_Metal_Calibre_0.18um.214a

7. If the file is executed successfully, a new .gds file for the dummy metal will be available under the folder, as well as a report file.

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+ Other Locations				

8. In CIW, click File -> New -> Library to create a new library for the dummy metal. Attach this library to the technology library **tsmc18**.

New Library			
Library Name dummy_filling_CS Directory (non-library directories)	Technology File Compile an ASCII technology file Reference existing technology libraries Attach to an existing technology library Do not need process information		
/home/hezm/ECE4220	No design manager setup found	alp	

9. In CIW, click File -> Import -> Stream to stream in the .gds file of the dummy metal. Also, make sure you load the layermap file.

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Stream File	9	/home/hezm/ECE	=4220/dummy_m -	etal_filling/dum	nmy_CS_amp	lifier.gds	
library		dummy_filling_CS	5				
lop Level (Jell	CS_amplifier					
Attach Tech	Track File	tsmc18					
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Note: the Top Level Cell name must be the same as the top level cell name of the **original** layout (not the dummy metal layout).

Note: for different PDKs and different environment setups, the location of the layermap may differ. If you cannot find it, talk to the TA.

- 10. Click **Translate**. Make sure there are no errors.
- 11. Under the **dummy_filling_CS** library, you should see a **layout** view.

Lib	orary Manager: WorkAr	ea: /home/hezm/ECE4220 _ 🗖	×	
Eile Edit View Design Manager Help cäden co				
Show Categories Library dummy_filling_CS Homework a1 analogLib avTech basic cdsDefTechLib dummy_filling_CS tsmc18	Show Files	View Iayout View ^ Lock Size	8k	
Messages Log file is "/home/hezm Beginning simple copy Processing files to be o	/ECE4220/libManager.log. to library "Homework". copied	10".		
2		Lib: dummy_filling_CS Free: 9.10	л	

- 12. You may open the **dummy metal layout** file to see how it actually look like. But as the circuit is very simple. You may not see things easily, which is fine.
- 13. Create a new layout to combine the original layout with the dummy metal layout

	New File ×
- File	
Library	dummy_filling_CS
Cell	CS_dummy_combined
View	layout
Туре	layout 🔽
Application	
Open with	Layout L 🔽
🔲 Always use th	his application for this type of file
Library path file	
/home/hezm/EC	E4220/cds.lib
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14. In **Layout Suite L Editing** window, create the instances of the layout for both the original layout and the dummy metal layout.

15. Open the **Property** of the instances for both the original layout and dummy metal layout, make their locations both **(0, 0)**.

		Edit	Instance Proper	ties		×
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	Cell	CS_amplifier			1	
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	Physical Only					
C	Convert To Mosaic			OK Cancel	Apply Hel	p

16. The dummy metal filling is done. Now you can generate a new .gds file and send this to a foundry for fabrication.